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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CAMPOS, YAIMA	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 11/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/750,567	MCALPINE ET AL.	
	Examiner	Art Unit	
	Yaima Campos	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

RESPONSE TO AMENDMENT

1. The examiner acknowledges the applicant's submission of the amendment dated August 21, 2006. At this point, claims 1, 2, 8, 17-23, 25-26, 30-33, 36, 38-42 and 46 have been amended, and no claims have been cancelled. There are 49 claims pending in the application; there are 7 independent claims and 42 dependent claims, all of which are ready for examination by the examiner.

I. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. **Claims 1-4, 8-13, 17, 20-24, 26, 33, 36, 38-42, 45-46 and 49** are rejected under 35 U.S.C. 102(b) as being anticipated by Langerman et al. (US 6,360,282).

4. As per **claim 1**, Langerman discloses "A machine-implemented method comprising:" "receiving, by a first process in a first virtual memory address space, a shortcut to a physical address associated with a level of a multi-level virtual address translation table;" **[With respect to this limitation, Langerman discloses a "Buffer Handle" (equivalents to Applicant's claimed shortcut) which "is used to identify a region of memory serving as a data buffer for an I/O request" (Column and Figures 4-6) and explains that once a memory region is registered to a user, "the Adapter Manager 32 returns a Buffer Handle to the user which**

includes the index of the CTE_PA (Context Translation Entry Physical Address) within the CTA_PA (Context Translation Array Physical Address)" (Column 6, lines 32-39). Langerman discloses "the interface employs a User Register Set (URS) 21 and an associated User Context Register Set (UCRS) 23... Each URS 21 is mapped into a corresponding region of the memory space of the CPU 11" (Col. 3, line 64-Col. 4, line 24) wherein "before a user may perform I/O to memory buffers, the virtual memory associated with the buffer must be registered with the Adapter Manager 32. Exemplary buffers are shown in Fig. 4, which shows two virtual memory regions that have been registered with the Adapter Manager 32" (Col. 6, lines 23-40)]

"posting a descriptor, the descriptor comprising a virtual address in the first virtual memory address space and the shortcut, to an interface between the first process and a second process, wherein the second process is in a second virtual memory address space;" **[Langerman discloses this limitation as "descriptors" wherein "the user posts I/O commands to a device by enqueuing descriptors on the Send Queue 24" (Column 4, lines 28-34) and explains that a virtual interface is a "structure of software interface presented to a user application for performing disk I/O" (Columns 3-4, lines 64-67 and 1-24, Column 7, lines 10-17 and Figure 2). Langerman discloses "the interface employs a User Register Set (URS) 21 and an associated User Context Register Set (UCRS) 23... Each URS 21 is mapped into a corresponding region of the memory space of the CPU 11" (Col. 3, line 64-Col. 4, line 24) wherein "before a user may perform I/O to memory buffers, the virtual memory associated with the buffer must be registered with the Adapter Manager 32. Exemplary buffers are**

shown in Fig. 4, which shows two virtual memory regions that have been registered with the Adapter Manager 32" (Col. 6, lines 23-40)]

"and determining, by the second process, the physical address corresponding to the virtual address based on at least the virtual address and the shortcut" **[With respect to this limitation, Langerman discloses using the "Buffer Handle" which has a pointer to a virtual memory region to access a "PAS (Physical Address Segment)" (Column 7, lines 27-34 and Figure 6)] See (Column 2-3, lines 30-67 and 1-12)].**

5. As per **claim 2**, Langerman discloses "The method of claim 1" **[See rejection to claim 1 above]** "further comprising transferring data to or from a buffer located at the physical address" **[With respect to this limitation, Langerman discloses "I/O request" performed to read or write from/to "data buffers" (Column 2, lines 52-65 and Figures 4-6)].**

6. As per **claim 3**, Langerman discloses "The method of claim 1" **[See rejection to claim 1 above]"** further comprising: generating the shortcut by a third process **[Langerman discloses this concept as a "user registers a memory region" and then "the Adapter Manager 32 returns a Buffer Handle to the user which includes the index of the CTE_PA (Context Translation Entry Physical Address) within the CTA_PA (Context Translation Array Physical Address)" (Column 6, lines 32-39) which comprise different processes].**

7. As per **claims 4, 17, 26, 33 and 36**, Langerman discloses "The method of claim 3" **[See rejection to claim 3 above]** wherein generating the shortcut by the third process comprises: generating/receiving a request to register a virtual buffer, the request including a virtual address corresponding to the start of the virtual buffer; **[With respect to this limitation, Langerman discloses that "before a user may perform I/O to memory buffers, the virtual memory**

associated with the buffer must be registered with the Adapter Manager 32" wherein "a user registers a memory region by specifying a virtual base address and a length" (Column 6, lines 23-39 and Figure 4)]

"determining the physical address of one level of the multi-level address translation table associated with the virtual memory space in which the virtual buffer resides;" **[With respect to this limitation, Langerman discloses "the Adapter Manager 32 creates an entry in the Context Translation Array-Physical Address (CTA_PA). Each entry in the CTA_PA is known as a Context Translation Entry-Physical Address (CTE_PA)" (Column 6, lines 23-39)]**

and generating a shortcut based on the physical address of the one level of the multi-level address translation table **[With respect to this limitation, Langerman discloses "The Adapter Manager 32 returns a Buffer Handle to the user which includes the index of the CTE_PA (Context Translation Entry Physical Address) within the CTA_PA (Context Translation Array Physical Address)" (Column 6, lines 32-39)]**. Additionally, Langerman discloses a computer system according to the invention which includes **["one or more CPUs 12" (Figure 1 and Column 3, lines 56-63)]** (As specified in claim 26)

a first process in a first virtual memory address space and a second process in a second virtual memory address space **Langerman discloses "the interface employs a User Register Set (URS) 21 and an associated User Context Register Set (UCRS) 23... Each URS 21 is mapped into a corresponding region of the memory space of the CPU 11" (Col. 3, line 64-Col. 4, line 24) wherein "before a user may perform I/O to memory buffers, the virtual memory associated with the buffer must be registered with the Adapter Manager 32.**

Exemplary buffers are shown in Fig. 4, which shows two virtual memory regions that have been registered with the Adapter Manager 32" (Col. 6, lines 23-40)]

wherein the interface is between the second process and the third process **[With respect to this limitation, Langerman discloses "the safe device access technique employs an abstracted device interface, as well as protection features to prevent an application program for accidentally or purposely damaging other application programs ... a virtual interface between the application program and the storage entity is then created. The virtual interface includes a queue for transmitting commands from the application program for the storage entity" (Col. 2, lines 30-51); therefore, the interface as described by Langerman comprises an interface "between" different applications/processes as claimed by Applicant]**

transmitting a request over a network to a third process in a second virtual memory address space to perform and input or output operation on the virtual buffer **[With respect to this limitation Langerman discloses "processing of input/output (I/O) requests to storage devices in computer systems" (Col. 1, lines 17-20) wherein "the technique may be used with storage entities other than disk drives. It may be used, for example with network file servers or similar remote storage devices" (Col. 9, lines 48-50)]**.

8. As per **claims 8, 21 and 38**, Langerman discloses "The method of claims 1, 20 and 36" **[See rejection to claims 1 and 36 above and claim 20 bellow]** "further comprising determining if the physical address is associated with the virtual address" **[Langerman discloses this concept as "when a descriptor is queued in a VI (virtual interface), the adapter verifies that the PTAG in the VI matches the PTAG in the CTE_PA that maps the user buffer identified in the descriptor" (Column 7, lines 10-17)]**.

9. As per **claims 9, 22 and 39**, Langerman discloses "The method of claims 1, 20 and 36" **[See rejection to claim 1 and 36 above and rejection to claim 20 bellow]** "further comprising determining if the virtual page containing the virtual address is pinned into physical memory" **[Langerman discloses this limitation as "Protection Tag or PTAG" which is used "to permit selective sharing of memory segments between a user application and an I/O device" (Column 7, lines 10-17)]**.

10. As per **claims 10, 45 and 49**, Langerman discloses "The method of claims 1, 42 and 46" **[See rejection to claim 1 above and claims 42 and 46 bellow]** "wherein the interface is a virtual interface" **[With respect to this limitation, Langerman discloses "virtual interface or VI, and as a safe device interface or SDI" (Columns 3-4, lines 64-67 and 1-24)]**.

11. As per **claims 11, 23 and 40**, Langerman discloses "The method of claims 1, 20 and 36" **[See rejection to claims 1 and 36 above and rejection to claim 20 bellow]** "further comprising determining if the first process is authorized to access the virtual address" **[Langerman discloses this limitation as "the adapter 16" verifies whether "a user has permission to use a user-specified region of memory to perform an I/O operation" (Column 7, lines 46-67)]**.

12. As per **claims 12, 24 and 41**, Langerman discloses "The method of claims 1 and 20" **[See rejection to claims 1 and 36 above and rejection to claim 20 bellow]** "further comprising determining if descriptors posted to the interface between the first process and second process are authorized to access the virtual address" **[Langerman discloses this concept as commands are sent to the adapter 16 using a descriptor 50 (Columns 8-9 lines 59-67 and 1-2 and Figure 8) wherein "it is verified that a user has access rights to a disk area identified in a disk read or write command" (Column 9, lines 14-36)]**.

13. As per **claim 13**, Langerman discloses "The method of claim 1" **[See rejection to claim 1 above]** "further comprising: receiving, by a first process, a plurality of shortcuts, each shortcut to a physical address associated with a level of a multi-level virtual address translation table" **[With respect to this limitation, Langerman discloses that a user registers a memory region to be able to perform I/O operations and in response, the Adapter Manager returns a Buffer Handle to the user wherein when a user registers a plurality of memory regions, a plurality of Buffer Handles (or shortcuts) will be returned to a user (Column 6, lines 31-32)]**.

14. As per **claim 20**, Langerman discloses "The method of claim 17 further comprising:" **[See rejection to claim 17 above]**

"and determining the physical address of the virtual address based on the virtual address and the shortcut, wherein the request includes the shortcut and a virtual address associated with the virtual buffer" **[With respect to this limitation, Langerman discloses posting descriptors every time an I/O is to be done and returning a "Buffer Handle" to a user (Columns 2-3, lines 52-67 and 1-12; Column 4, lines 28-49; Columns 8-9, lines 59-67 and 1-2; Figure 8)] the "Buffer Handle" has a pointer to a virtual memory region to access a "PAS (Physical Address Segment)" (Column 7, lines 27-34 and Figure 6)] See (Column 2-3, lines 30-67 and 1-12)]**.

15. As per **claims 42 and 46**, Langerman discloses "A system comprising:"

"a client computer;" or "storage device" **["host computer 10" which includes "system memory 14" and I/O adapters 16 (Columns 3-4, lines 56-67 and 1-24 and Figure 1)]**

"and a server in communication with the client computer using a network, the server comprising:" **[Langerman discloses this limitation in (Columns 3-4, lines 56-67) and explains that "the segment-based translation and protection mechanism described above is targeted towards a dedicated server applications such as databases or embedded applications that usually control the majority of the resources of the server" (Column 8, lines 1-4)]**

"a first processor capable of producing a shortcut to a physical address associated with a level of a multi-level virtual address translation table and writing a descriptor comprising a virtual address and the shortcut to an interface;" **[With respect to this limitation, Langerman discloses Langerman discloses this limitation as "descriptors" wherein "the user posts I/O commands to a device by enqueuing descriptors on the Send Queue 24" (Column 4, lines 28-34) and explains that a virtual interface is a "structure of software interface presented to a user application for performing disk I/O" (Columns 3-4, lines 64-67 and 1-24, Column 7, lines 10-17 and Figure 2) wherein a "Buffer Handle" (equivalent to Applicant's claimed shortcut) which "is used to identify a region of memory serving as a data buffer for an I/O request" (Column and Figures 4-6) and "is passed to the adapter 16 in a descriptor" (Column 7, lines 35-36).** Langerman also discloses a computer system according to the invention which includes **["one or more CPUs 12" (Figure 1 and Column 3, lines 56-63)]** and a second processor capable of performing operations in a second virtual memory address space, the operations including **[Langerman discloses "the interface employs a User Register Set (URS) 21 and an associated User Context Register Set (UCRS) 23... Each URS 21 is mapped into a corresponding region of the memory space of the CPU 11" (Col. 3, line 64-**

Col. 4, line 24) wherein "before a user may perform I/O to memory buffers, the virtual memory associated with the buffer must be registered with the Adapter Manager 32. Exemplary buffers are shown in Fig. 4, which shows two virtual memory regions that have been registered with the Adapter Manager 32" (Col. 6, lines 23-40)] reading the descriptor posted on the interface, determining a physical address of the virtual address based on at least the virtual address and the shortcut and transferring data located at the physical address to the client computer using the network **[Langerman discloses this limitation as using a "Buffer Handle" which has a pointer to a virtual memory region to access a "PAS (Physical Address Segment)" (Column 7, lines 27-34 and Figure 6)] See (Column 2-3, lines 30-67 and 1-12). Also see Columns 2-3, lines 30-67 and 1-12; Columns 6-7, lines 23-67 and 1-45)** ***To further explain, Langerman discloses "the technique may be used with storage entities other than disk drives. It may be used, for example, with network file servers or similar remote storage devices" (Col. 9, lines 45-57)***].

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. **Claims 5-7, 14-16, 18-19, 25, 27-32, 34-35, 37, 43-44 and 47-48** are rejected under 35 U.S.C. 103(a) as being unpatentable over Langerman et al. (US 6,360,282) in view of Arndt (US 2003/0204648).

18. As per **claims 5-7, 14-16, 18-19, 25, 27-28, 34-35, 37, 43-44 and 47-48**, Langerman discloses the method of claims 1, 4, 17, 26, 33, 36, 42 and 46 **[See rejection to claims 1, 4, 17, 26, 33, 36, 42 and 46 above]** wherein processes have different virtual memory address spaces **[Langerman discloses "the interface employs a User Register Set (URS) 21 and an associated User Context Register Set (UCRS) 23... Each URS 21 is mapped into a corresponding region of the memory space of the CPU 11" (Col. 3, line 64-Col. 4, line 24) wherein "before a user may perform I/O to memory buffers, the virtual memory associated with the buffer must be registered with the Adapter Manager 32. Exemplary buffers are shown in Fig. 4, which shows two virtual memory regions that have been registered with the Adapter Manager 32" (Col. 6, lines 23-40)]** but does not disclose expressly using a function/key to encrypt "the shortcut" which is unknown to a first/client process wherein only the host/second process is capable of decrypting said key.

Arndt discloses using function/key to encrypt "the shortcut" which is unknown to a first/client process wherein only the host/second process is capable of decrypting said key as **["a method, apparatus, and program for sharing logical resources among separate partitions in a logically partitioned data processing system" (Page 1, Paragraph 0002) wherein an "opaque handle" refers to an entity "which cannot be directly de-reference by the untrusted agents" thereby protecting shared resources against "untrusted agents" (Pages 4, Paragraphs 0036-0038 and Figure 3). Arndt also explains that "the hosting (client) partition uses the hypervisor function, called H_PUT RTCE, which takes as a parameter the opaque handle of the RTCE (Remote Translation Control Entry) table, such as RTCE table 330" (Page 4, Paragraph 0036) wherein only the client partition has access to the**

RTCE table but not the TCE (Translation Control Entry) which belongs to the host partition and maps to physical addresses. The client partition is provided and opaque handle to perform I/O operations within the host partition's memory space; therefore, preventing the client partition from containing references to a physical address of a logical resource that belongs to the host partition (Page 4, Paragraph 0042; Page 5, Paragraph 0046)].

Langerman et al. (US 6,360,282) and Arndt (US 2003/0204648) are analogous art because they are from the same field of endeavor of computer memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the method of processing I/O requests to storage devices in a computer system which uses shortcuts/handles taught by Langerman and use a function/key to encrypt "the shortcut" which is unknown to a first/client process wherein only the host/second process is capable of decrypting said key as taught by Arndt.

The motivation for doing so would have been because Arndt discloses use a function/key to encrypt "the shortcut" which is unknown to a first/client process wherein only the host/second process is capable of decrypting said key provides **[protection for memory resources as "by resistant to forging, the opaque handle has the characteristic such that an untrusted agent is unlikely to be able to generate, by itself, a value that would be interpreted by the hypervisor as a valid opaque handle to a TCE table" wherein the hypervisor could tell if "some other agent was trying to forge a handle to a TCE table" (Page 4, Paragraph 0038)]**.

Therefore, it would have been obvious to combine Arndt (US 2003/0204648) with Langerman et al. (US 6,360,282) for the benefit of creating a method/system to control I/O

requests to shared storage devices to obtain the invention as specified in claims **5-7, 14-16, 18-19, 25, 27-28, 34-35, 37, 43-44 and 47-48**.

19. As per **claim 29**, the combination of Langerman and Arndt discloses "The system of claim 28" **[See rejection to claim 28 above]** "wherein the instructions of the third process cause the second processor to determine if the physical address is associated with the second process" **[Langerman discloses this concept as "when a descriptor is queued in a VI (virtual interface), the adapter verifies that the PTAG in the VI matches the PTAG in the CTE_PA that maps the user buffer identified in the descriptor" (Column 7, lines 10-17)]**.

20. As per **claim 30**, the combination of Langerman and Arndt discloses "The system of claim 28" **[See rejection to claim 28 above]** "wherein the instructions of the third process cause the second processor to determine if the associated virtual pages associate with the physical address are pinned into physical memory" **[Langerman discloses this limitation as "Protection Tag or PTAG" which is used "to permit selective sharing of memory segments between a user application and an I/O device" (Column 7, lines 10-17)]**.

21. As per **claim 31**, the combination of Langerman and Arndt discloses "The system of claim 28" **[See rejection to claim 28 above]** "wherein the instructions of the third process cause the second processor to determine if the second process is authorized to access the virtual buffer" **[Langerman discloses this limitation as "the adapter 16" verifies whether "a user has permission to use a user-specified region of memory to perform an I/O operation" (Column 7, lines 46-67)]**.

22. As per **claim 32**, the combination of Langerman and Arndt discloses "The system of claim 27" **[See rejection to claim 27 above]** "wherein the instructions of the third process cause

the second processor to determine if requests posted to the interface between the second process and the third process are to authorized access the virtual buffer" **[Langerman discloses this concept as commands are sent to the adapter 16 using a descriptor 50 (Columns 8-9 lines 59-67 and 1-2 and Figure 8) wherein "it is verified that a user has access rights to a disk area identified in a disk read or write command" (Column 9, lines 14-36)]**.

IV. RELEVANT ART CITED BY THE EXAMINER

1. The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See **MPEP 707.05(c)**.

2. The following reference teaches having translation tables to isolate an application's memory from another's.

U.S. PATENT NUMBER

US 7,082,507

V. ACKNOWLEDGMENT OF ISSUES RAISED BY THE APPLICANT

Response to Amendment

23. Applicant's arguments filed on August 21, 2006 have been fully considered and are not persuasive.

24. As required by **M.P.E.P. § 707.07(f)**, a response to these arguments appears below.

VI. ARGUMENTS CONCERNING PRIOR ART REJECTIONS

1st POINT OF ARGUMENT:

25. With respect to Applicant's remarks that Langerman does not disclose posting a descriptor to an interface between a first process and a second process in different virtual memory address spaces as Langerman's interface is a software interface supporting multiple concurrent users for I/O, it is the Examiner's position that Langerman's disclosure meets all the limitations as required by the broadest reasonable interpretation of the claim language **[Langerman discloses "the interface employs a User Register Set (URS) 21 and an associated User Context Register Set (UCRS) 23... Each URS 21 is mapped into a corresponding region of the memory space of the CPU 11" (Col. 3, line 64-Col. 4, line 24) wherein "before a user may perform I/O to memory buffers, the virtual memory associated with the buffer must be registered with the Adapter Manager 32. Exemplary buffers are shown in Fig. 4, which shows two virtual memory regions that have been registered with the Adapter Manager 32" (Col. 6, lines 23-40); therefore, each user has a different register set mapped to a different virtual region. Furthermore, Langerman discloses "the safe device access technique employs an abstracted device interface, as well as protection features to prevent an application program for accidentally or purposely damaging other application programs ... a virtual interface between the application program and the storage entity is then created. The virtual interface includes a queue for transmitting commands from the application program for the storage entity" (Col. 2, lines 30-51); therefore, the interface as described by Langerman comprises an interface "between" different applications/processes as claimed by Applicant]**.

2nd POINT OF ARGUMENT:

26. With respect to Applicant's remarks that a single user in Langerman cannot constitute different processes, it is the Examiner's position that **["The user posts I/O commands to a device by enqueuing descriptors on the Send Queue 24" (Col. 4, lines 18-34) which comprise different processes and also explains having multiple applications and users (Col. 8, lines 11-14) which comprise different processes, a user/application is able to process/execute different commands and processes]**.

3rd POINT OF ARGUMENT:

27. With respect to Applicant's remarks that Langerman does not disclose data transfer between different processes and that Langerman does not disclose data transfer over a network, it is the Examiner's position that Langerman's disclosure meets these limitations as **[With respect to this limitation Langerman discloses "processing of input/output (I/O) requests to storage devices in computer systems" (Col. 1, lines 17-20) wherein "the technique may be used with storage entities other than disk drives. It may be used, for example with network file servers or similar remote storage devices" (Col. 9, lines 48-50)]**.

28. All arguments by the applicant are believed to be covered in the body of the office action; thus, this action constitutes a complete response to the issues raised in the remarks dated August 21, 2006.

VII. CLOSING COMMENTS

Conclusion

29. **THIS ACTION IS MADE FINAL**. Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. 1.136(a).

A shortened statutory period for reply to this final action is set to expire three months from the mailing data of this action. In the event a first reply is filed within **two months** of the mailing date of this final action and the advisory action is not mailed until after the end of the **three-month** shortened statutory period, then the shortened statutory period will expire on the data the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing data of the advisory action. In no event, however, will the statutory period for reply expire later than **six months** from the mailing date of the final action.

VIII. STATUS OF CLAIMS IN THE APPLICATION

30. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. § 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

31. Per the instant office action, **claims 1-49** have received a second action on the merits and are subject of a final rejection.

32. For at least the above reasons it is the examiner's position that the applicant's claims are not in condition for allowance.

IX. DIRECTION OF ALL FUTURE REMARKS

33. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yaima Campos whose telephone number is (571) 272-1232. The examiner can normally be reached on Monday to Friday 8:30 AM to 5:00 PM.

IMPORTANT NOTE

34. If attempts to reach the above noted Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Sanjiv Shah, can be reached at the following telephone number: Area Code (571) 272-4098.

35. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

October 27, 2006

Yaima Campos
Examiner
Art Unit 2185

SANJIV SHAH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100